ASCIA - A Multi-Vendor IC Design System

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Abstract

The semiconductor division of Siemens AG is one of the major global players in the semiconductor business. Goals like globalization, innovation, cost reduction and enhancement of productivity and quality require an excellent design system for integrated circuits. The IC CAD system “ASCIA” was developed by Siemens Semiconductor’s central CAD department. It consists of a set of proprietary concepts (“ASCIA kernel”) plus tools from a multitude of suppliers plus proprietary technology and library data.
The three main sections of this paper present
- the architecture of the most recent ASCIA version
- the role of Cadence’s software in it and
- a short summary of our Opus 4.4 beta test.

1 Introduction

1.1 Siemens Halbleiter

With an annual turnover of about DM 5 Billion, the semiconductor division “Siemens Halbleiter” (abbr. “HL”) of the german Siemens AG is one of the top 20 semiconductor companies worldwide. In europe, HL is among the top 3 in semiconductor sales.

1.2 ASCIA

For all steps of the development cycle of integrated circuits, the IC design system “ASCIA” was developed by HL. Besides this “broadline” system, other CAD environments exist within HL for special purposes.
“ASCIA” stands for “Advanced Silicon CompIlAtion”. ASCIA is aimed at supporting design of analogue, digital and mixed-signal ICs in more than 30 bipolar, CMOS and BiCMOS technologies using full-custom or cell-based design methodology. Worldwide, about 1000 designers are working with ASCIA.

The first generation (1.X) of ASCIA was initially released in 1990. It was a “best tool in market” approach. The effort for system integration was very high and the CAD department had to write and maintain a lot of “glue” software. Key tools were bought from Mentor (e.g. design entry, digital simulation), Cadence (layout verification, P&R) and Analogy. ASCIA 1.4 comprises about 700 MByte of programs and data. This ASCIA generation is still used by several hundred designers in Munich and in HL’s other development centers worldwide.

In order to cut down CAD efforts and improve design productivity, it was decided to focus on one supplier for a state-of-the-art CAD system. As a broadliner and EDA technology leader, Cadence was chosen as partner. The result was HL’s “fourth generation” IC CAD system called ASCIA 4.X. Developed purely for in-house purposes, its first version 4.1 was initially released in December 1994. Since then, new components or component versions are officially released in a new ASCIA 4.1.X subversion once per month.

2 Architecture of ASCIA 4.1

In the following subsections, the term “ASCIA” relates to ASCIA 4.1.

2.1 Hardware/Software Platform

Currently, ASCIA is available for Sun workstations running SunOS 4.1.3. The GUI used is OpenWindows 3.

2.2 System Integration and Software Distribution

ASCIA is developed by HL’s central IC CAD department in Munich, Germany. Since 1995, Siemens HL started many IC development cooperations with other companies. In order to make library and design data exchange as easy as possible, it was decided that many of these companies should receive the ASCIA 4.1 kernel software plus HL-specific technology and library data needed for their projects. This meant that HL’s CAD system integration group found themselves in the role of a distributor of highly complex and individual software. The process of adapting ASCIA 4.1 to this new situation is still going on.
From Munich, the whole system, flow specific parts of it or just design kits for one technology are distributed to over 20 locations worldwide including HL’s design centers and various external design contractors. Because we found no commercial tool satisfying our requirements, we are developing the “OpenDist” /1/ software for effective distribution of our CAD software within Siemens’ worldwide corporate network.

2.3 System Structure

ASCIA consists of versioned “packages”. I.e. each tool bundle (like all the Cadence or all the Synopsys software), all technologies and libraries and all SKILL code units may exist in several versions in the system in parallel. For each released package, a “current” version exists which points to the most recent release. All program packages are activated using the “modules” /2/ software. The complete ASCIA 4.1 installation with all available package versions comprises about 30 GByte of programs and data.
In order to facilitate installation of ASCIA components and co-existence of ASCIA with other design systems, we try so separate “original” software from ASCIA-specific extensions. Nevertheless, we often need to apply minor changes to the “commercial” software to link it to ASCIA.
In the Munich “master installation”, all ASCIA software is stored on central file servers and made available at the user workstations via NFS and automounter. All user and design data is stored locally on the workstations.

2.4 Design Project Structure

Each ASCIA 4.1 project owns a special UNIX account and a UNIX group with the name of the project. Below the home directory of such a project account, all data belonging to the design is stored in a predefined directory structure. It allows to work in an arbitrary number of subprojects and within each subproject in an arbitrary number of versions. In each subproject version, tool specific directories exist which store the tool specific data. Below such a directory, each user

may create his/her own working directory. Also, each subproject version contains ASCIA-specific configuration files which store default parameters and information about the tool/technology/reference library/SKILL-package versions to be used. Of each package, either a fixed version or the version “current” may be chosen.

2.5 User Roles, Access Rights

In ASCIA 4.1, we have defined two “user roles”: the “designer” and the “project administrator”. If a designer shall become member of a project’s team, the project’s UNIX group is added to the UNIX group list of that user. Which means that one user may be member in up to 15 project teams. Project administrators are defined via entries in the project account’s “.rhosts” file. A person may play both ASCIA roles.

All ASCIA 4.1 users first have to log in to their personal account and afterwards switch to a project account of their choice using the ASCIA command “set_project”. It is not possible to directly log in to project accounts. In the project environment, designers work with umask 007, project admins with umask 027. The task of a project admin is to set up and maintain the project structure and the configuration files and to define the project team. A project admin does not have the environment to execute design related tasks. If a designer enters a subproject version in a project account, the environment is automatically configured according to the entries in the configuration files and the project’s UNIX group is made the primary group of the user. This means all design data in a project account belongs to the same UNIX group, but individual users. People who are not members of the project team do not have access to the project’s data.

2.6 Automatic Design Environment Configuration

When a design tool is executed in the ASCIA environment, the command issued by the user usually invokes a wrapper script which automatically generates (most of) the tool specific setup data from the ASCIA specific configuration files. Afterwards, the tool is started. Wherever possible, we have implemented a hierarchical tool initialization sequence: after global, ASCIA-specific configuration data, the subproject version specific configuration data is evaluated. Finally, if it exists, user specific configuration data is processed. This concept provides a very high degree of flexibility but requires some care.

2.7 Documentation

Because the Cadence and the Synopsys online documentation were both based on the same tool, we decided to also use Interleaf for the ASCIA 4.1 online documentation and offer all three documentations within one interface. Cadence’s shift back to Framemaker was another reason for us to migrate to HTML.

2.8 Information Tools

Within the Siemens intranet, we offer additional information tools to the ASCIA user community: A hotline tool based on “Sun Call Tracker”. It allow users to easily report bugs and enhance-

ment requests to the responsible component administrator in the CAD department.
In various HL-specific “news” groups, we spread highly actual information about new ASCIA features and bugs which were discovered in released components.

2.9 Quality Management

The CAD department has to spend high effort in testing the “commercial” software as well as the proprietary parts of ASCIA. We usually perform a three phase test cycle with a component: test in the development environment (only for proprietary parts), a “stand-alone” test of the component in the system environment and finally, a test of the partial flow(s) the component is part of. The test report which is written for each component has to be accepted by a “built-in quality” circle and the QA manager. The whole release process is controlled by our hotline tool.

3 The Cadence Software in ASCIA

One of the fundamental changes from ASCIA 1.X to ASCIA 4.X was the introduction of Cadence’s DFII and the CDBs. In the initial release of ASCIA 4.1, we were offering an “ASCIA 1.4 emulation” flow which contained almost all “old” ASCIA 1.4 tools. Our original plan was to remove as many non-Cadence tools as possible from ASCIA 4. But meanwhile, we have tools from about 10 vendors in our system.

In the following sections, the term “Opus” will be used for the Cadence IC design tool suite while “DFII” will be used for the “pure” design framework which only contains the common software infrastructure like GUI, DM, IPC, SKILL etc.

3.1 Quality Assurance

In the past, we have released new Opus versions as soon as possible after having completed our internal tests. Currently, we are using the 4.3.4 release. The process of testing the Opus software components, filing PCRs, integrating bugfixes and re-testing requires up to 6 months (elapsed time). We are never releasing the software configuration of Opus we get on CDs but always a configuration which was enhanced by integrating various hotfixes. We feel that our QA effort for the Cadence tools is comparatively high compared with other tools we use.
A problem for the CAD department and CAD system administrators is the structural complexity and low degree of modularity of the Cadence software. Whenever a serious bug is found somewhere in an Opus component which we have released in ASCIA, we have to duplicate the whole Opus package (about 1.5...2 GByte) and add the hotfix tar kit(s) to the new package version in order to guarantee that each released package version remains unchanged. We would like to have the DFII monolith split up into small chunks which we can integrate, test and release separately without unknown side-effects. This should be easy to accomplish with “stand alone” tools like Leapfrog, Verilog, CDC, Cell3, Dracula, Vampire, etc.

3.2 Opus Configuration

In ASCIA, the Cadence tools are configured and functionally enhanced using SKILL code. When the DFII is started in the ASCIA project environment, a hierarchical initialization

sequence is performed. The toplevel ".cdsinit" file first loads some generic ASCIA-specific code. Afterwards, it evaluates the subproject specific ASCIA configuration files and pre-configures the DFII accordingly. Things automatically set are e.g. the default technology file and the library search path. All SKILL packages specified are loaded. Afterwards, a subproject version specific and a user specific ".cdsinit" file are loaded in case they exist. One problem we face is the ".cdsenv" file which is always stored in and loaded from a fixed location (the user's home directory). This can lead to problems in case a designer works in several different projects which would require different ".cdsenv" file contents.

3.3 Our SKILL Packages

ASCIA contains over 90,000 lines of SKILL code in almost 50 packages. The main purposes of our SKILL packages are
- (partly flow specific) tool configuration, e.g. for Composer, Virtuoso, Verilog, Spectre
- configuration of the DFII's CDB design management
- implementation of a hierarchical power supply concept including proprietary netlisters and necessary tool specific functional extensions (e.g. for Composer and P&R tools)
- implementation of a user friendly backannotation flow
- implementation of a simple documentation facility for CDB data
- graphical encapsulation of most of ASCIA's non-Cadence tools into the DFII
- implementation of various utilities for administration and manipulation of CDB data

We find SKILL extremely powerful and consider it one of the best features of Opus. We have developed our own SKILL style guide and SKILL naming conventions. We would appreciate very much a style guide checking program.

3.4 CDB Data Management

In ASCIA, we only store those views in CDBs which cannot be stored directly in the UNIX file system (e.g. schematic, symbol, layout, abstract, ...). For example, we are not storing our VHDL data in CDBs but in the tool specific directories mentioned above.
A big problem in ASCIA is corruption of CDB data. In case an Opus tool crashes or the connection of a user workstation to its software server is lost for several seconds, we frequently get inconsistent or even completely destroyed CDBs and we have almost no repair utilities.
We sometimes faced problems with "cdsd" which probably got confused in our automounter environment where we used machine aliases. Cadence's introduction of the "filehost" and "filepath" CDB properties resulted in so many user complaints that we had to deactivate their evaluation. Why didn't Cadence spend any effort in a simple UI which allows easy adjustment of the new properties even for inexperienced designers? This would surely have been beneficial for the whole Cadence user community. It should not be considered a matter of individual implementation or consulting work.
Many of our users, mainly the analogue and memory product designers, want to be able to work with configurations of design data. Because configurations of CDB data don't work properly and due to the fact that we store many views outside CDBs, we are using the versioning concept of ASCIA to implement this feature.

3.5 Advanced Design Management Features

When we planned ASCIA 4.1, we asked our users whether they wanted any kind of design flow management including “flow charts” as a nice, intuitive user interface. The answer was “Yes, as an option.” We found out that we could not guarantee data consistency with the functionality available in the DFII at that time and had to drop the plan. A generic flow management would also require that all tools which can be run without user interaction (like netlisters and simulators) can be activated without starting the DFII’s GUI.
As an effect of the globalization of HL’s business, we face more and more projects with globally distributed design teams. The DFII’s DM does not help us with this.
Because a large portion of our digital chips are designed using VHDL, we need a VHDL code control system which knows about the semantics and inner structure of the code and facilitates development work by providing a “make”-like mechanism. For the second task (and more), some of our VHDL designers use Runtime Design Automation’s design tracing system VOV.

3.6 Documentation and Training Classes

A complex system needs good educational aids. The less intuitive it is to use, the easier the access to needed information must be. We find the DFII’s online help system very helpful. The value of the openbook online documentation could be enhanced by adding more links between related information. We would appreciate if functional hotfixes of the software were instantly reflected in the online documentation.
Within HL, hundreds of designers are using the Cadence tools in the ASCIA environment. Therefore, we need user training courses which are adapted to our project setup, libraries and design methodologies. Because ASCIA supports various different design flows which include tools from many vendors, we need additional flow-oriented training. We are spending much effort to fulfill these user requirements.

3.7 IP Protection and Data Security Aspects

ASCIA 4.1 is no longer an in-house system. Selected parts of our technology and library data as well as lots of SKILL code have to be delivered to companies which are not 100% owned by Siemens. How can Cadence help us protect our intellectual property? “Normal” SKILL code can be converted to context files. What about technology data in “.tf” files and verification runsets?

UNIX is an inherently insecure operating system. It is relatively easy to become “root” and thus gain illegal access to design data. While this problem may be beyond the scope of an EDA tool supplier we expect a CAD system supplier to offer solutions and/or expertise.

4 Some OPUS 4.4 Beta Test Results

Because many tool related enhancement of Opus will be implemented in version 4.4, we would like to introduce it as soon as possible.

At the end of 1995, we were invited by Cadence Munich to take part in the Opus 4.4 beta test. The beta test was carried out at Siemens HL in Munich in January and February 1996. We were

mainly working with version 4.4.194. In the following three sections, we focus the items which have the biggest impact on the CAD department and our users.

4.1 CDB Conversion

We expect the new 5.X CDB architecture to resolve the main problems we currently face with CDBs: DB inconsistency/corruption, missing administrative utilities, multi-user edit- and hierarchical access performance, poor structure and protection of the technology related data.

Because the CAD department can't take over the task of converting thousands of CDBs from 4.3 to 4.4 format, we need an automatic solution for our users. Cadence's “libcvt” procedure worked without problems during our tests and thus seems to be a good kernel for a complete migration tool set.

4.2 SKILL Code Conversion

Before we can release Opus 4.4.X in ASCIA, we have to migrate almost all the ASCIA 4.1 SKILL code (except the DM packages) plus all user-written code to 4.4. During our beta test, we were using 4.4 SKILL lint and Cadence’s migration hints to convert several of our SKILL packages. We found that SKILL lint, or a related tool, needs enhancement in three areas:
1) All obsolete functions should have hints for replacement.
2) Statistics need to be generated when there is a large body of code to help assess the magnitude of the conversion job.
3) Invalid CDB object attribute references need to be detected. The problem is that the attributes of the CDB design objects have changed in some cases, and 4.4 SKILL lint does not find these.

4.3 TDM

We have the impression that customizing TDM for use in ASCIA and getting our designer to accept this tool will be the biggest effort in our Opus 4.4 migration plan. Currently, we expect to broadly release Opus 4.4.X in ASCIA not earlier than mid 1997.

TDM provides the basic features needed for design management, but the performance makes it questionable whether it is usable in a real design environment. For the SKILL development, we could use all of the features successfully. Because some TDM commands are implemented as shell scripts calling sed, awk, split and sort, they are slow and potentially unreliable. For either the technology libraries or design project libraries, the number of cells would overload the advanced functions. With the current implementation, we consider using just the basic checkin/checkout functions of TDM for versioning of cell data. TDM obviously contains no component for management of projects whose data is globally distributed. It would have been useful for the TDM documentation to have some discussion on how to partition projects and choose the correct structure.

5 Outlook

The number of tool vendors required to build a broadline, leading-edge IC CAD system will continue to grow. We have chosen Cadence as our primary supplier and would like to use as many Opus tools as possible. But good tools and libraries aren't sufficient to ensure high productivity of the designers. Items like a “smooth” flow, consistent and intuitive user interfaces and powerful design data management functions are not less important.

Currently, we are currently migrating ASCIA 4.1 to Solaris 2.5. Our next milestone is to release Opus 4.4.X in a new major ASCIA version, 4.2. We have chosen a multi-step approach:
First, we will replace the DM functionality we presently have with an equivalent TDM solution. (This means TDM will handle only CDBs.)
In case our users accept TDM, we will in a second step put all design data under TDM control.
The third step will mean implementation of advanced design management functionality like support of globally distributes design teams, design flow management and a coupling to design project management tools.
We are waiting for a commitment and a roadmap from Cadence to support such framework-related features, maybe through integration of existing commercial products into their system.

A framework must *per definitionem* be an open, modular system. On the other hand, nobody can expect any company to widely open its doors to its competitors. We want to use the DFII as a central part of our CAD system. This clearly means that third parties must be able to easily integrate (not necessarily graphically) their tool(s) into the Cadence framework. The DFII as a an “exclusive” framework for the Cadence tools wouldn’t make much sense for us.

References

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Short Biography

Name:
Thomas Harriehausen (pronounced Harry-how-sen) was born in 1958

Company:
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Job Title:
Leader CAD systems integration group (since July 1995),
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Job Description:
Within the central CAD department, responsible for the following aspects of the IC design system ASCIA:
- system architecture
- integration of technology & library data and tools
- quality management
- software distribution worldwide
- data and CAD system security
- system documentation
- user training
- design data management
- DFII configuration and user support

Education background:
Finished studies of electrical engineering and computer science at University of Hannover in 1987 with M.S. degree. Diploma work about automatic generation of resistor layouts for bipolar ICs.
In 1992, Ph.D. thesis about adaptive real-time network simulation.